CLAIMS

1. A semiconductor device comprising:

a semiconductor chip upon which are disposed roughly upon a straight line a plurality of bonding pads containing a first region as a connection region and a second region for making contact with a testing probe, and said first and second regions are lined up in a direction perpendicular to said straight line,

a member provided with a plurality of conductors containing a third region as a connection region electrically connected to each of a plurality of external connection terminals and a securing area for securing said semiconductor chip,

a plurality of conductor wires that electrically connect said first regions of said plurality of bonding pads to said third regions of said plurality of conductors, and

an encapsulating member that encapsulates said semiconductor chip and said plurality of conductor wires.

2. The semiconductor device according to claim 1 wherein said plurality of bonding pads comprise first bonding pads provided with said first regions toward the edge of said semiconductor chip and second bonding pads provided with said second regions toward the edge of said semiconductor chip, and said first and second bonding pads are disposed alternately roughly upon a straight line.

3. The semiconductor device according to claims 1 or 2 wherein said plurality of bonding pads are rectangular in shape with their with their short sides lying in a direction along the edges of said semiconductor chip.

4. The semiconductor device according to claims 1 or 2 wherein said plurality of bonding pads are formed with the width of said first region being wider than the width of said second region in the direction along the edges of said semiconductor chip.

5. The semiconductor device according to claims 1 or 2 wherein said plurality of bonding pads have notches between said first region and said second region.

6. The semiconductor device according to any of claims 1, 2, 3, 4 or 5 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

7. A method of manufacturing semiconductor devices comprising:

a step wherein a semiconductor chip upon which are disposed roughly upon a straight line a plurality of bonding pads containing a first region as a connection region and a second region for making contact with a testing probe, and said first and second regions are lined up in a direction perpendicular to said straight line, and a member provided with a plurality of conductors containing a third region as a connection region electrically connected to each of a plurality of external connection terminals and a securing area for securing said semiconductor chip are secured, and

a step wherein a plurality of conductor wires electrically connect said first regions of said plurality of bonding pads to said third regions of said plurality of conductors.

8. The method of manufacturing semiconductor devices according to claim 7 wherein said plurality of bonding pads comprise first bonding pads provided with said first regions toward the edge of said semiconductor chip and second bonding pads provided with said second regions toward the edge of said semiconductor chip, and said first and second bonding pads are disposed alternately roughly upon a straight line.

9. The method of manufacturing semiconductor devices according to claim 8 wherein said connection step comprises: a first step wherein said first region of said plurality of first bonding pads are connected by conductor wire to said third regions of said plurality of conductors, and a second step wherein said first region of said plurality of second bonding pads are connected by conductor wire to said third regions of said plurality of conductors.

10. The method of manufacturing semiconductor devices according to any of claims 7, 8 or 9, further comprising a step wherein, prior to said securing step, testing of said semiconductor chip is performed by putting test probes into contact with the second regions of said plurality of bonding pads.

the aforementioned QFP, etc., the terminating end of the conductor wire may be bonded to inner leads. In addition, in a semiconductor device containing a plurality of semiconductor chips, the lands may also be the bonding pads of other semiconductor chips.

Moreover, the process of the embodiment illustrated the case in which the bonding to the first pads, namely the bonding pads that have the bonding region on the outside, was first completed and then the bonding to the second pads, namely the bonding pads that have the bounding region on the inside, was performed. However, as long as the present invention is followed, it is also possible to perform bonding of the first pads and second pads alternately starting from the edge of the semiconductor chip. In addition, at the time of working of the present invention, the shape of the bonding pads is not limited to the aforementioned embodiments, but rather they may also be trapezoidal in shape.

Effects of the Invention

By means of the present invention as described above, the region of the bonding pad to which the conductor wire is bonded will not be damaged by the contact of probes in the previous inspection step, and accordingly, the reliability of connection of conductor wires to the bonding pads is not decreased.

In addition, according to the present invention wherein the orientation of bonding regions alternates among adjacent bonding pads, it is possible to make the pitch between bonding positions on adjacent bonding pads greater than the pitch between bonding pads, and accordingly, the pitch between bonding pads can be made smaller in spite of the inline layout of bonding pads.

CLAIMS

1. A semiconductor device comprising:

a semiconductor chip upon which are disposed roughly upon a straight line a plurality of bonding pads containing a first region as a connection region and a second region for making contact with a testing probe, and said first and second regions are lined up in a direction perpendicular to said straight line,

a member provided with a plurality of conductors containing a third region as a connection region electrically connected to each of a plurality of external connection terminals and a securing area for securing said semiconductor chip,

a plurality of conductor wires that electrically connect said first regions of said plurality of bonding pads to said third regions of said plurality of conductors, and

an encapsulating member that encapsulates said semiconductor chip and said plurality of conductor wires.

2. The semiconductor device according to claim 1 wherein said plurality of bonding pads comprise first bonding pads provided with said first regions toward the edge of said semiconductor chip and second bonding pads provided with said second regions toward the edge of said semiconductor chip, and said first and second bonding pads are disposed alternately roughly upon a straight line.

3. The semiconductor device according to claims 1 or 2 wherein said plurality of bonding pads are rectangular in shape with their with their short sides lying in a direction along the edges of said semiconductor chip.

4. The semiconductor device according to claims 1 or 2 wherein said plurality of bonding pads are formed with the width of said first region being wider than the width of said second region in the direction along the edges of said semiconductor chip.

5. The semiconductor device according to claims 1 or 2 wherein said plurality of bonding pads have notches between said first region and said second region.

6. The semiconductor device according to any of claims 1, 2, 3, 4 or 5 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

7. A method of manufacturing semiconductor devices comprising:

a step wherein a semiconductor chip upon which are disposed roughly upon a straight line a plurality of bonding pads containing a first region as a connection region and a second region for making contact with a testing probe, and said first and second regions are lined up in a direction perpendicular to said straight line, and a member provided with a plurality of conductors containing a third region as a connection region electrically connected to each of a plurality of external connection terminals and a securing area for securing said semiconductor chip are secured, and

a step wherein a plurality of conductor wires electrically connect said first regions of said plurality of bonding pads to said third regions of said plurality of conductors.

8. The method of manufacturing semiconductor devices according to claim 7 wherein said plurality of bonding pads comprise first bonding pads provided with said first regions toward the edge of said semiconductor chip and second bonding pads provided with said second regions toward the edge of said semiconductor chip, and said first and second bonding pads are disposed alternately roughly upon a straight line.

9. The method of manufacturing semiconductor devices according to claim 8 wherein said connection step comprises: a first step wherein said first region of said plurality of first bonding pads are connected

by conductor wire to said third regions of said plurality of conductors, and a second step wherein said first region of said plurality of second bonding pads are connected by conductor wire to said third regions of said plurality of conductors.

10. The method of manufacturing semiconductor devices according to any of claims 7, 8 or 9, further comprising a step wherein, prior to said securing step, testing of said semiconductor chip is performed by putting test probes into contact with the second regions of said plurality of bonding pads.